Chettinad College of Engineering & Technology
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Academic Year 2024-25

Question Bank

Year/Semester: III/ V	**Department :ECE**	**Unit : I/II/III/IV/V**
Date:12/08/2024	**Subject Code/Title :EC3552 VLSI and chip design**	**Section : Part A/B/C**
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UNIT I-MOS TRANSISTOR PRINCIPLES

PART A

1. Define threshold voltage of a MOSFET. (R)

The threshold voltage of a MOSFET is usually defined as the gate voltage where an inversion layer forms the interface between the insulating layer (oxide) and the substrate (body) of the transistor.

2. What is enhancement mode FET? (R)

A type of FET in which there are no charge carriers present in the channel, when the gate voltage is in zero. In these devices, the increasing the gate voltage will increases the current flow from source to drain.

3. What specifications you will consider for selecting a MOSFET? (R)

- Breakdown voltages
- Forward transconductance
- Drain source on resistance (Rds)
- Switching characteristics
- Zero gate voltage drain current (Idss)
- Input capacitance (Ci)

4. Give the major advantages of IC. (R)

- Size is less
- High speed
- Less power dissipation.

5. What are different generations of integration circuits? (R)

- SSI (Small Scale Integration)
- MSI (Medium Scale Integration)
- LSI (Large Scale Integration)
- VLSI (Very Large Scale Integration).

6.Give the variety of integrated circuits (ICs).

- More Specialized Circuits (MSC).
- Application Specific Integrated Circuits (ASICs).
- Systems on Chips (SOC).

7.What are the different terminals in MOS transistors? (R)

- Drain
- Source
- Gate.

8.What is depletion mode operation MOS? (R)

If the channel is initially doped lightly with p-type impurity a conducting channel exists at zero gate voltage and the device is said to operate in depletion mode.

9.What are the two types of mode of operation of MOSFET? (R)

- Enhancement mode
- Depletion mode

10.What is enhancement mode operation of MOS? (U)

If the gate field must induce a channel before current can flow and the gate voltage enhances the channel current and such a device is said to the enhancement mode MOS.

11. What is latch up? (U)

Latch up is a condition in which the parasitic components give rise to the establishment of low resistance conducting paths between VDD and VSS with disastrous results. Careful control during fabrication is necessary to avoid this problem.

12. State the advantages of CMOS process. (R)

- Low power dissipation
- High packing density
- Bidirectional capability
- Low input impedance
- Low delay sensitivity to load.

13. State the different operating regions for an MOS transistor. (U)

- Cut-off region
- Non-saturated region
- Saturated region.

14. Define threshold voltage of CMOS.

The threshold voltage, Vt for a MOS transistor can be defined as the voltage applied between the gate and the source of the MOS transistor below which the drain to source current, IDS effectively drops to zero.

15. What is body effect?

The threshold voltage VT is not a constant with respect to the voltage difference between the substrate and the source of MOS transistor. This effect is called substrate- bias effect or body effect.

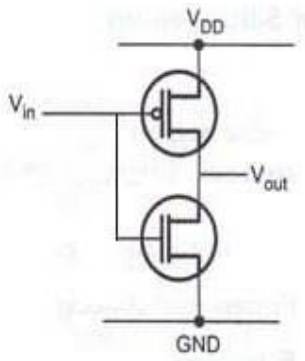
16. What is channel length modulation?

The current between drain and source terminals is constant and independent of the applied voltage over the terminals. The effective length of the conductive channel is actually modulated by the applied voltage VDS, increasing VDS causes the depletion region at the drain junction to grow, reducing the length of the effective channel.

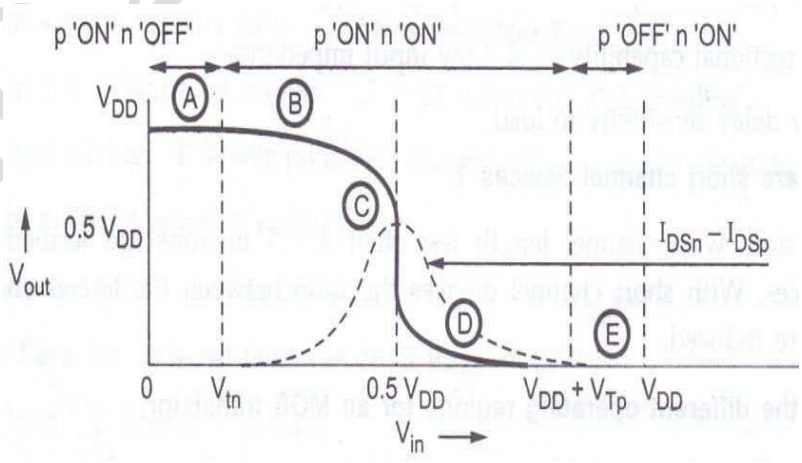
17. Why NMOS technology is preferred than PMOS technology?

N channel transistors have greater switching speed when compared to PMOS transistors.

18. Draw the basic CMOS inverter circuit.



19. Give the CMOS inverter D.C. transfer characteristics and operating regions.



20.Compare PMOS and NMOS

PMOS	NMOS
Current conduction is due to the Holes	Current conduction is due to the electrons
Less switching speed due to lower mobility of holes	Higher switching speed due to greater mobility of electrons
Transistor width is higher	Transistor width is lower
PMOS transistors have greater resistance generally in the range of 2R-3R.	It has lower resistance because of its reduced transistor width.

21. Compare enhancement mode and depletion mode MOSFET.

Enhancement MOSFET	Depletion MOSFET
Device that is normally cut off with zerogate bias is called as enhancement MOSFET	Device that conducts with zero bias iscalled depletion MOSFET
Channel is induced by the gate voltage for current conduction	It has defused channel for current conduction
It operates in enhancement mode only	It operates on enhancement as well as depletion mode.

Part B

1. Explain the structure and working of nMOS and pMOS transistor. **(13) (A)**
2. Summarize the following using CMOS logic: **(U)**
   (i) Inverter with truth table **(6)**
   (ii) NAND Gate with truth table**.(7)**
3. Illustrate with necessary diagrams **(A)**
   (i) Ideal I-V characteristics of MOS transistors**.(6)**
   (ii) C-V characteristics of MOS transistors.**(7)**
4. Discuss in detail about the velocity saturation and channel length modulation. **(13) (U)**
5. Write short notes on: **(R)**
   (i) Body Effect**,(4)**
   (ii) Subthreshold Condition,**(4)**
   (iii) Junction Leakage**.(5)**
6. Interpret the DC transfer characteristics of CMOS inverter. **(13) (A)**
7. Describe the following with necessary equations. **(U)**
   Detailed MOS gate capacitance model,**(7)**
   Detailed MOS diffusion capacitance model.**(6)**
8. Write short notes on: **(R)**
   (i) Transistor scaling.**(7)**
   (ii) Interconnect scaling**.(6)**
9. Design a CMOS inverter and formulate the beta ratio effects and noise margin**.(13) (C)**

Part C

1. Explain MOS resistance and inductance in detail. **(15) (U)**
2. Write a brief description about choosing the best number of stages to minimize delay large network. **(15) (U)**

3. Compare the constant field and constant voltage scaling approaches in terms of area ,delay,energy and power density parameters. **(15) (U)**
4. Explain the basic concepts of supply voltage scaling. **(15) (U)**
5. How the latch up problem can be overcome? **(15) (AZ)**

UNIT II-COMBINATIOAL LOGIC CIRCUITS

Part A

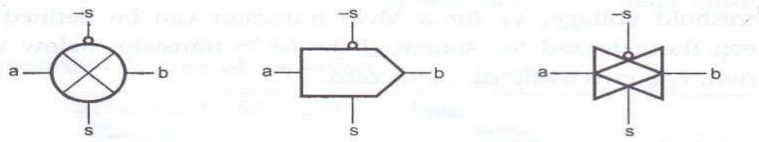
1.What is a pull down device? (R)

A device connected so as to pull the output voltage to the lower supply voltage usually 0 V is called pull down device.

2.What is pull up device? (R)

A device connected so as to pull the output voltage to the upper supply voltage usually VDD is called pull up device.

3.Give the different symbols for transmission gate. (R)



4.What is mean by power and power dissipation? (R)

Power is the rate at which energy is delivered or exchanged; power dissipation is the rate at which energy is taken from the source (VDD) and converted into heat (electrical energy is converted into heat energy during operation).

5.What is mean by PDP? (R)

- Power delay product (PDP) = Pav * t p = (CL V2)/2
- PDP is the average energy consumed per switching event (watts * sec = joule).

6.What is EDP? (R)

- Energy delay product (EDP) = PDP* tp = Pav *tp2
- EDP is the average energy consumed multiplied by the computation time required.

7.What are two types of power dissipation? (R)

- Static dissipation due to leakage current or other current drawn continuously from the power supply.
- Dynamic dissipation due to
- a)Switching transient current.
- b)Charging and discharging of load capacitances.

8.Define elmore delay model. (U)

It is an analytical method used to estimate the RC delay in a network. Elmore delay model estimates the delay of a RC ladder as the sum over each node in the ladder of the resistance Rn-1 between that node and a supply multiplied by the capacitor on the nodes.

9.What are the general properties of elmore delay model? (R)

- General property of Elmore delay model network has Single input node. All the capacitors are between a node and ground .
- Network does not contain any resistive loop

10.What is static power dissipation? (R)

The power dissipation due to leakage current when the MOS transistor is in idle state is called the static power dissipation. Static power due to Sub threshold conduction through OFF transistors Tunneling current through gate oxide. Leakage through reverse biased diodes Contention current in radioed circuits.

11.What is dynamic power dissipation? (R)

Power dissipation is due to circuit switching to charge and discharge the output load capacitance at a particular node at operating frequency is called dynamic power dissipation.

12.What are the methods available to reduce dynamic power dissipation? (U)

- Reducing the product of capacitance and its switching frequency.
- Eliminate logic switching that is not necessary for computation.
- Reduce activity factor Reduce supply voltage

13.What are the methods to reduce static power dissipation? (U)

- By selecting multi threshold voltages on circuit paths with low-Vt transistors while leakage on other paths with high-Vt transistors.
- By using two operating modes, active and standby for each function blocks.
- By adjusting the body bias (i.e) adjusting FBB (Forward Body Bias) in active mode to increase performance and RBB (Reverse Body Bias) in standby mode to reduce leakage.
- By using sleep transistors to isolate the supply from the block to achieve significant leakage power savings.

14.What is short circuit power dissipation? (R)

During switching, both NMOS and PMOS transistors will conduct simultaneously and provide a direct path between VDD to ground resulting in short circuit power dissipation.

15.Define Design margin. (U)

The additional performance capability above required standard basic system parameters that may be specified by a system designer to compensate for uncertainties is called design margin. Design margin required as there are three sources of variation two environmental and one manufacturing.

16.Write the applications of transmission gate? Multiplexing element of path selector. (U)

- A latch element an unlock switch
- Act as a voltage controlled resistor connecting the input and output.

17.What is pass transistor? (R)

It is a MOS transistor, in which gate is driven by a control signal, when the control signal is high, input is passed to the output and when the control signal is low, the output is floating topology such topology circuits is called pass transistor.

18.List the advantages of pass transistor logic. (U)

- Pass transistor logic circuits are often superior to standard CMOS circuits in terms of layout density, circuit delay and power consumption.
- They do not have path VDD to GND and do not dissipate standby power (static power dissipation).

19.What is transmission gate? (R)

The circuit constructed with the parallel connection of PMOS and NMOS with shorted drain and source terminals. The gate terminal uses two select signals s and □̄, when s is high than the transmission gate passes the signal on the input. The main advantage of transmission gate is that it eliminates the threshold voltage drop.

20.What are the various ways to reduce the delay time of a CMOS inverter? (R)

- The width of the MOS transistor can be increased to reduce delay this is known as gate sizing, which will be discussed later in more details.
- The load capacitance can be reduced to reduce delay this is achieved by using transistor of smaller and smaller dimension by feature generation technology.
- Delay can also be reduced by increasing the supply voltage VDD and reducing the threshold voltage Vt of the MOS transistors

21.What is stick diagram? (R)

It is used to convey information through the use of color code. Also it is the cartoon of a chip layout.

22.What are the uses of stick diagram? (R)

- It can be drawn much easier and faster than a complex layout.
- These are especially important tools for layout built from large cells.

23.Give the various color coding used in stick diagram. (U)

- Green - n-diffusion
- Red - Polysilicon
- Blue - Metal
- Yellow - Implant
- Black - Contact areas.

24. What makes dynamic CMOS circuits faster than static CMOS circuits? (R)

As MOS dynamic circuits require lesser number of transistors and capacitance is to be driven

by it. This makes MOS dynamic circuits faste

Part B

1. Analyse the following static CMOS logic. **(AZ)**
   (i) Bubble pushing **(4)**
   (ii) Compound gates **(4)**
   (iii) Skewed gates. **(5)**
2. Illustrate the following circuits in detail. **(A)**
   (i) Pseudo-Nmos. **(8)**
   (ii) Ganged CMOS. **(5)**
3. Explain in detail about Cascade voltage switch logic. **(U)**
4. Write short notes on **(R)**
   (i) Domino logic**. (7)**
   (ii) (ii) Dual-rail Domino Logic. **(6)**
5. Draw the 2-input multiplexers using the following circuittechniques**.(C)**
   (iii)Static CMOS. **(4)**
   (iv)Pseudo-Nmos. **(4)**
   (v) CVSL. **(5)**
6. Summarize the following. **(U)**
   (i) Pass transistor logic. **(7)**
   (ii) (ii) Complementary pass transistor logic. **(6)**
7. Evaluate the design of Differential Cascade Voltage Switch with Pass Gate**.(E)**
8. Describe in detail about the following. **(U)**
   (iii)Keepers. **(5)**
   (iv)Multiple-Output Domino Logic (MODL). **(4)**
   (v) NP and Zipper Domino. **(4)**
9. Manipulate the various Rationed circuits for CMOS circuits. **(13) (A)**
10. Discuss the structure and working of CMOS with Transmission gates. **(13) (U)**
11. Construct the various low-power reduction techniques**. (13) (C)**
12. Summarize the following. **(U)**
    (i) Input ordering delay effect. **(7)**
    (ii) Asymmetric gates,P/N ratios. **(6)**
13. Evaluate the following Dynamic circuits **.(E)**
    (i) Domino logic. **(5)**
    (ii) Dual-rail Domino logic. **(4)**
    (iii) Keepers. **(4)**
14. Evaluate the following Dynamic circuits**. (13) (E)**
15. Formulate the following power dissipation in CMOS circuits. **(C)**
    (i) Static dissipation. **(8)**
    (ii) Dynamic dissipation. **(5)**

Part C

1. Write short notes on **(R)**
   (i) Noise margin. **(5)**
   (ii) Rise Time. **(5)**
   (iii) Fall Time. **(5)**
2. Compare CMOS and bipolar technology. **(15) (U)**
3. Explain in detail about the scaling concept and its fundamental limits. **(15) (U)**
4. Derive an expression for the rise time,fall time, and propagation delay of a CMOS inverter. **(15) (A)**
5. Explain in detail about low power design principles. **(15) (U)**

UNIT III-SEQUENTIAL LOGIC CICUITS AND CLOCKING STRATEGIES

Part A

1.What is metastability and list the steps to prevent it? (R)

Metastability is an unknown state it is neither zero nor one. Metastability happens for the design systems violating setup or hold time requirements. Setup time is a requirement that the data has to be stable before the clock edge and hold time is a requirement that the data has to be stable after the clock edge. The potential violation of the setup and hold violation can happen when the data is purely asynchronous and clocked synchronously.

Steps to prevent metastability:

- Using proper synchronizers (two stage or three stage), as soon as the data is coming from the asynchronous domain. Using synchronizers, recovers from the metastable event.
- Use synchronizers between cross-clocking domains to reduce the possibility from metastability.
- Using faster flip flops (which has narrower metastable window).

2.What is the difference between mealy and moore state machines? (R)

In the mealy state machine we can calculate the next state and output both from the input and state. But in the moore state machine we can calculate only next state but not output from the input and state and the output is issued according to next state.

3.What is the difference between latches and flip-flops based designs? (U)

Latches are level-sensitive and flip-flops are edge sensitive. Latch based design and flop based design is that latch allows time borrowing which a tradition flip-flop does not: That makes latch based design more efficient. But at the same time, latch based design is more complicated and has more issues in min timing (races).

4.What are the classifications of CMOS circuit families? (R)

- Static CMOS circuits.
- Dynamic CMOS circuits. Ratioed circuits.
- Pass-transistor circuits.

5.What are the characteristics of Static CMOS design? (R)

A static CMOS circuit is a combination of two networks, one is pull-up network (PUN) and the other is pull-down network (PDN) in which at every point in time, each gate output is connected to either VDD or VSS via pull-up or pull down network.

6.List the important properties of Static CMOS design. (R)

- At any instant of time, the output of the gate is directly connected to VDD and VSS.
- The function of the PUN is providing a connection between the output and VDD.
- The function of the PDN is providing a connection between the output and VSS.

- Both PDN and PUN are constructed in mutually exclusive way such that one and only one of the networks is conduct in steady state. That is, the output node is always a low-impedance node in steady state.

7.What is Dynamic CMOS logic? (R)

Dynamic circuits rely on the temporary storage of signal values on the capacitance of high impedance node. It requires only N+2 transistors. It takes a sequence of precharge and conditional evaluation phases to realize the logic functions.

8.What are the properties of dynamic logic? (R)

- Logic function is implemented by pull-down network only.
- Full swing outputs (VOL= GND and VOH = VDD).
- Non-ratioed.
- Faster switching speeds.
- Needs a precharge clock.

9.What are the disadvantages of dynamic CMOS technology? (R)

A fundamental difficulty with dynamic circuits is a loss of noise immunity and a serious timing restriction on the inputs of the gate. Violate monotonicity during evaluation phase.

10.What is CMOS Domino logic? (R)

A static CMOS inverter placed between dynamic gates which eliminate the monotonicity problem in dynamic circuits are called CMOS Domino logic.

11.What is called static and dynamic sequencing element? (U)

A sequencing element with static storage employs some sort of feedback to retain its output value indefinitely. A sequencing element with dynamic storage generally maintains its value as charge on a capacitor that will leak away if not refreshed for a long period of time.

12.What is clock skew? (R)

In reality clocks have some uncertainty in their arrival times that can cut into the time available for useful computation. It is called clock skew.

13.What are synchronizers? (R)

Synchronizers are used to reduce metastability. The synchronizers ensure synchronization between asynchronous input and synchronous system.

14.Difference between latches and Flip-Flop. (U)

S.No	Latch	Flip-Flop
1.	A Latch is Level Sensitive	A flip-flop is edge triggered.
2.	A latch stores when the clock level is low and is transparent when the level is high.	A flip-flop stores when the clock rises and is mostly never transparent.

15.Define Pipelining. (R)

Pipelining is a popular design technique often used to accelerate the operation of the data path in digital processors. The major advantages of pipelining are to reduce glitch in complex logic networks and getting lower energy due to operand isolation.

16.How the limitations of a ROM based realization is overcome in a PLA based realization. (AZ)

In a ROM, the encoder part is only programmable and use of ROMs to realize Boolean functions is wasteful in many situations because there is no cross-connect for a significant part. This wastage can be overcome by using Programmable Logic Array (PLA), which requires much lesser chip area.

17.What is static 0 hazard? (R)

Output goes momentarily 1 when it should remain at 0 is called static 0 hazard.

18.Define propagation delay and contamination delay? (R)

- Propagation delay: The amount of time needed for a change in a logic input to result in a permanent change at an output that is the combinational logic will not show any further output changes in response to an input change.
- Contamination delay: The amount of time needed for a change in a logic input to result in an initial change at an output, that is the combinational logic is guaranteed not to show any output change in response to an input change before fed time units have passed.

19.Define Setup time and Hold time. (R)

- Setup time (tsetup): The amount of time before the clock edge that data input D must be stable the rising clock edge arrives.
- 20.Hold time (thold): This indicates the amount of time after the clock edge, the data input D must be held stable in order for Flip Flop to latch the correct value. Hold time is always measured from the rising clock edge to a point after the clock edge

Part B

1. Explain the inverting property of full adder. **(13) (U)**
2. How to design a column multiplexer with separate decoder circuit? **(13) (AZ)**
3. Write the full adders output in terms of propagate and generate. **(13) (U)**
4. Discuss in detail: **(U)**
   (i) Master-Slave Edge-Triggered Register**. (7)**
   (ii) Timing properties of Multiplexer-Based Master-Slave registers. **(6)**
6. Write short notes on: **(U)**
   (i) Multiplexer-Based Latches. **(8)**
   (ii) Low-Voltage Static Latches. **(5)**
7. Explain the C2MOS Register with CLK- CLK clocking approach.**(13) (U)**
8. Evaluate the True Single-Phase Clocked Register (TSPCR) and TSPC Edge-Triggered register. **(13) (E)**
9. Illustrative the following Alternative Register styles,Pulse Register,Sense-Amplifier-Based

Registers. **(13) (A)**

11. Classify the various Pipelining techniques and explain in detail. **(13) (U)**
12. Summarize the following. **(U)**
    (i) Latch versus Register based pipeline. **(6)**
    (ii) NORA-CMOS logic style for pipelined structures. **(7)**
13. Define Schmitt trigger and its properties. **(13) (R)**
14. Describe Schmitt trigger and its CMOS implementation with neat diagram. **(13) (U)**
15. Construct the clock-distribution techniques dealing with clock skew and jitter. **(13) (C)**
16. Describe in detail: **(U)**
    (i) Synchronous interconnect.**(4)**
    (ii) Mesochronous interconnect.**(3)**
    (iii) Plesiochronous interconnect.**(3)**
    (iv) Asynchronous interconnect.**(3)**
17. Examine the Monostable Sequential circuits and Astable circuits with neat an example.**(13) (U)**
18. Analyze the basics of synchronous timing, clock skew, clock jitter and combined impact of skew and jitter. **(13) (AZ)**
19. Manipulate the various sources of skew and jitter. **(13) (U)**
20. Evaluate the Master-Slave Edge-Triggered register with estimating properties and Non-ideal clock signals. **(13) (E)**

Part C

1. Summarize the following: **(U)**
   (i) Dynamic transmission-gate edge-triggered registers. **(5)**
   (ii) C2MOS-A clock-skew insensitive approach. **(5)**
   (iii) True single-phase clocked register. **(5)**
2. Formulate the following Nonbistable sequential circuits. **(C)**
   (i) The Schmitt Trigger. **(5)**
   (ii) Monostable Sequential Circuits. **(5)**
   (iii) Astable Circuits. **(5)**
3. Design the clock distribution strategies for three generations of the digital alpha Microprocessors. **(C)**
4. Illustrate the principles of synchronizer and arbiter. **(A)**
5. Explain in detail about the pipelining concept used in sequential circuits **(U)**

UNIT IV-INTERCONNECT , MEMORY RCHITECTURE AND ARITHMETIC

Part A

1.How data path can be implemented in VLSI system? (AZ)

A data path is best implemented in a bit-sliced fashion. A single layout is used repetitively for every bit in the data word. This regular approach eases the design effort and results in fast and dense layouts

2.Write short note on the performance of ripple carry adder. (U)

A ripple carry adder has a performance that is linearly proportional to the number of bits. Circuit optimizations concentrate on reducing the delay of the carry path. A number of circuit topologies exist proving that careful optimization of the circuit topology and the transistor sizes helps to reduce the capacitance on the carry bit

3.What are the advantages of ripple carry adder? (R)

- Circuit realization is very simple Consumes less power
- Compact layout giving smaller chip area

4.What is carry skip adder? (R)

A carry skip adder consists of a simple ripple carry adder with a special speed up carry chain called a skip chain. The carry skip circuitry consists of two logic gates. The AND gate accepts the carry in bit and compares it to the group propagate signal.

5.What is mirror adder? (R)

In this circuit realization the PMOS network is identical to the NMOS network rather than being the conduction complement, so the topology is called a mirror adder.

6.What are the advantages of carry skip adder? (R)

The propagation delay is smaller compare to ripple carry adder when optimal stages are used. The carry skip adder is shown to be superior to constant width carry skip module the advantages being greater at high precisions.

7.What is the logic of adder for increasing its performance? (R)

Other adder structures use logic optimizations to increase the performance (carry- bypass, carry select, carry look ahead). Performance increase comes at the cost of area.

8.What is a multiplier circuit? (R)

A multiplier is nothing more than a collection of cascaded adders. Critical path is far more complex and optimizations are different compared to adders.

9.Define input ordering. (R)

For PMOS and NMOS the inner inputs encounters the body effect and requires high threshold voltage to turn on. By input ordering the rare changing inputs are moved to inner inputs. This provides sufficient power saving.

10.Which factors dominates the performance of a programmable shifter? (R)

The performance and the area of a programmable shifter are dominated by the wiring.

11.Write down the expression for worst case delay for RCA. (U)

$$T = (n-1)\ tc+ts$$

12.Write down the expression to obtain delay for N-bit carry bypass adder. (U)

Tadder = tsetup +M*tcarry +(N/M-1)*tbypass +(M-1)*tcarry + tsum

13.Why we go for booth's algorithm? (AZ)

Booth logorithm is a method that will reduce the number of multiplicand multiples. For a given number of ranges to be represented, a higher representation radix leads to fewer digits.

14.List the different types of shifter. (R)

- Array shifter
- Barrel shifter
- Logarithmic shifter

15.What are the various shift operations available? (R)

- Logical left shift
- Logical right shift
- Arithmetic left shift
- Arithmetic right shift

16.What is the output after two arithmetic right shift for A=1001? (R)

- Input = 1001
- After first arithmetic right shift = 1100
- After second arithmetic right shift= 1110

17.What is a Manchestor carry chain adder? (R)

It uses a cascade of pass transistors to implement the carry chain. Propogate & generate signals are generated using pass transistor logic. The capacitance per node on the carry chain is very small & equals only 4 diffusion capacitances.

18.Why is carry bypass Adder called so? (AZ)

When the bypass control signal is set to '1', the incoming carry is forwarded immediately to the next block through a bypass transistor.

19.What is the importance of linear carry select Adder? (R)

The linear dependencies present in a ripple carry adder is avoided in linear carry select adder, by anticipating both possible values of the carry i/p and evaluate the result for both possibilities in advance.

20.Why is the propagation delay in a carry select Adder is linearly proportional to N? (AZ)

It is because the block select signal that selects between 0&1 solutions still has to ripple

through all stages in worst case.

21.What is a bit serial multiplier? (U)

When area is of prime concern, it is possible to reduce the cost of the multiplier by using a time multiplexed approach .Here, a combination of a single adder & a storage element is used to iteratively compute the summation of the partial products.

22.Differentiate DRAMs from SRAMs. (U)

Both SRAMs and DRAMs are volatile in nature, ie. Information is lost if power line is removed. However SRAMs provide high switching speed, good noise margin but require large chip area than DRAMs.

23. Explain the read and write operations for a one transistor DRAM cell. (U)

A significant improvement in the DRAM evolution was to realize 1-T DRAM cell. One additional capacitor is explicitly fabricated for storage purpose. To store '1', it is charged and to store '0' it is discharged to '0' volt. Read operation is destructive. Sense amplifier is needed for reading. Read operation is followed by restoration operation

Part B

1. (i) Describe ripple carry adder and derive the expression for worst case delay.**(8) (U)**
   (ii)Write a note on Carry Bypass adders.**(5) (R)**
2. Examine the concept of carry look ahead adder and discuss its types. **(13) (R)**
3. Outline the operation of a basic 4 bit adder. Describe the different approaches of improving the speed of the adder. **(13) (R)**
4. Illustrate the concepts of faster decoder and sum-addressed decoder circuit. . **(13) (AZ)**
5. Define SRAM memory cell operation and summarize short note on **(R)**
   (i) Read operation. **(7)**
   (ii) Write operation.**(6)**
6. Demonstrate the bit line conditioning circuitry with necessary circuit diagram.**(13) (U)**
7. Design a multiplier for 5 bit by 3 bit. Explain its operation and summarize the number of adders. **(13) (R)**
8. Discuss it over Wallace multiplier.**(13) (U)**
9. Summarize the Multi-ported SRAM and Register file CMOS Logic circuit. **(13) (U)**
10. Evaluate the architecture of large memory array with sub array memory Circuitry. **(13)(E)**
11. Give a note on linear carry select adder. **(13) (R)**
12. Examine the operation of : **(U)**
    (i) Static CMOS adders. **(7)**
    (ii) Mirror adder.**(6)**
13. Analyze the operation of booth multiplication with suitable examples. Justify how booth algorithms speed up the multiplication process. **(13) (AZ)**
14. Discuss the data paths in digital processor architectures. **(13) (U)**
15. Write detailed note about any two multiplier circuit. **(13) (R)**

Part C

1. Give a brief note a ripple carry adders. **(15) (R)**
2. Describe about carry look-ahead adder and its carry generation and propagation. **(15) (U)**
3. Write short note on Braun multiplier and Wallace tree multiplier. **(15) (R)**
4. Explain with neat diagram baugh-wooley multiplier. **(15) (U)**
5. Explain in detail about high speed adders. **(15) (U)**

UNIT V-ASIC DESIGN AND TESTING

Part A

1.What is the standard cell based ASIC design? (R)

A cell based ASIC (CHIC) uses predesigned logic cells known as standard cells. The standard cell areas also called flexible blocks in a CHIC are built of rows of standard cells. The ASIC designer defines only the placement of standard cells and interconnection in a CHIC. All the mask layers of a CHIC are customized and are unique to a particular customer.

2.What is a FPGA? (R)

A Field Programmable Gate Array (FPGA) is a programmable logic device that supports implementation of relatively large logic circuits. FPGAs can be used to implement a logic circuit with more than 20,000 gates whereas a CPLD can implement circuits of up to about 20,000 equivalent gates.

3.What are the different methods of programming of PALS? (R)

- Fusible links
- UV - Erasable EPROM
- EEPROM (E2PROM) - Electrically Erasable Programmable ROM.

4.What is an antifuse? (R)

An antifuse is normally high resistance (>100 MW). On application of appropriate programming voltages, the antifuse is changed permanently to a low resistance structure (200-500 W).

5.What are the different levels of design abstraction at physical design? (R)

- Architectural or functional unit
- Register Transfer level (RTL) Logic level
- Circuit level

6.What are programmable Interconnects? (R)

In a PAL, the device is programmed by changing the characteristics if the switching element. An alternative would be to program the routing.

7.What are the types of ASICs? (R)

- Full custom ASICs
- Semi custom ASICs

8.What are the types of programmable devices? (R)

- Programmable logic structure Programmable
- Interconnect Reprogrammable Gate Array

9.What are the features of standard celled ASICs? (R)

All mask layers are customized-transistors and interconnect. Custom blocks can be embedded Manufacturing lead time is about eight weeks.

10. What are the characteristics of FPGA? (U)

None of the mask layers are customized a method of programming the basic logic cells and the interconnect. The core is a array of programmable basic logic cells that can implement combinational as well as sequential logic (flip flops). A matrix of programmable interconnect surrounds the basic logic cells. Design turnaround is a few hours.

11. What is programmable logic array? (R)

A programmable logic array (PLA) is a programmable device used to implement combinational logic circuits. The PLA has a set of programmable AND planes, which link to a programmable OR planes, which can then be conditionally complemented to produce an output. This layout allows for a large number of logic functions to be synthesized in the sum of products canonical forms.

12. What is meant by programmable logic plane? (R)

The programmable logic plane is programmable read only memory (PROM) array that allows the signals present on the devices pins to be routed to an output logic macro cell.

13. Define ROM. (R)

A read only memory (ROM) is a device that includes both the decoder and the OR gates within a single IC package. It consists of n input lines and m output lines. Each bit combination of the input variables is called an address. Each bit combination that comes out of the output lines is called a word. The number of distinct addresses possible with n input variables is 2n.

14. What is the full custom ASIC design? (U)

In a Full custom ASIC, an engineer designs some or all of the logic cells, circuits and layout specifically for one ASIC. It makes sense to take this approach only if there are no suitable existing cell libraries available that can be used for the entire design.

15. Why was PAL developed? (AZ)

PAL was developed to overcome certain disadvantages of PLA, such as longer delays due to additional fusible links that result from using two programmable arrays and more circuit complexity.

16. State the types of ROM Masked ROM. (R)

- Programmable Read only Memory
- Erasable Programmable Read only memory.
- Electrically Erasable Programmable Read only Memory.

17.List the major differences between PLA and PAL PLA. (R)

- Both AND and OR arrays are programmable and Complex Costlier than PAL
- PAL AND arrays are programmable OR arrays are fixed Cheaper and Simpler

20.What are the steps involved in twin tub process? (R)

- Tub formation
- Thin oxide construction
- Source and drain implantation
- Contact cut definition
- Metallization.

21.What are the advantages of silicon on insulator (SOI) process? (R)

- No latch-up
- Due to absence of bulks transistor structures are denser than bulk silicon.

22.Give the different types of ASIC. (R)

- Full custom ASICs
- Semicustom ASICs Standard cell based ASICs Gate-array based ASICs
- Programmable ASICs Programmable Logic Device (PLD)
- Field Programmable Gate Array (FPGA).

23. State the different types of CMOS processes. (R)

- p-well process
- n-well process
- Silicon on insulator process
- Twin tub process

Part B

1. Explain the general architecture of FPGA and clearly bring out the different programmable blocks used. **(13) (U)**
2. Write the significance of PLA/FSM in VLSI design. **(13) (R)**
3. With neat sketch explain the CLB,IOB and programmable interconnects of an FPGA device. **(13) (R)**
4. What are the building blocks of XILINX CPLD?Explain the functional description of each block. **(13) (R)**
5. Discuss in detail about full custom design,semi-custom design. **(13) (U)**
6. Descibe bout Gate-Array-Based ASICs. **(13) (U)**
7. Write short note on Programmable Logic Devices. **(13) (R)**
8. Explain the concept of various technologies to programming FPGA. **(13) (U)**
9. Write shorts notes on standard cell design and cell libraries. **(13) (R)**
10. Explain the fabrication of PMOS transistor and its substrate fabrication process. **(13) (U)**
11. Explain p-well fabrication process of CMOS inverter. **(13) (U)**
12. Explain the electrical properties of MOS transistor in detail. **(13) (U)**

13. Explain twin-tub process of CMOS fabrication in detail. **(13) (U)**
14. Explain SOI process of CMOS fabrication in detail. **(13) (U)**
15. Explain N-well fabrication process in detail. **(13) (U)**

Part C

1. Explain about automatic test pattern characteristics. **(13) (U)**
2. Write the notes on Adhoc testing, Built in self-test. **(13) (R)**
3. Define Logic verification principles. **(13) (R)**
4. Discuss the detail about ASIC design flow. **(13) (U)**
5. Explain the Triple -well process. **(13) (U)**

Faculty Incharge **Head of the Department**

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